# PATENT ABSTRACTS OF JAPAN

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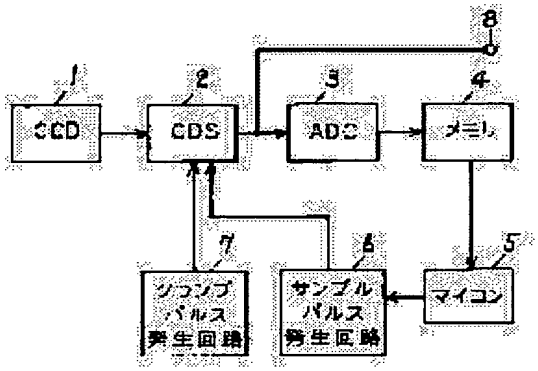
## (54) CORRELATION DUPLEX SAMPLING DEVICE

(57)Abstract:
PURPOSE: To optimize the phase of a sample pulse supplied to a correlation duplex sampling circuit (CDS circuit) through the use of a memory and a microcomputer and to obtain the image pickup signal of a high S/N.
CONSTITUTION: CCD 1 outputs a signal obtained by photoelectrically converting light into an electric signal and a CDS circuit 2 processes the output signal of a CCD 1. An ADC circuit 3 AD-converts the output signal of the CDS circuit 2, and the memory 4 stores the output signal of the ADC circuit and outputs stored data to the microcomputer. The microcomputer 5 supplies a phase control signal for controlling the phase of the sample pulse supplied to the CDS circuit 2 to a sample pulse generation circuit 7 based on the output signal of the memory. A sample pulse generation circuit 6 outputs the sample pulse supplied to the CDS circuit 2 based on the phase control signal supplied from the microcomputer 5. A clamping pulse generation circuit 7 generates a clamping pulse clamping the DC level of field through except for the reset pulse of the output signal from CCD 1, which is supplied to the CDS circuit 2.

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[Claim(s)]

[Claim 1] CCD which outputs the signal which carried out photo electric conversion of the light to the electrical signal using the lens etc. to a CDS circuit, The CDS circuit which is a correlation duplex sampling circuit which processes the output signal of said CCD, The ADC circuit which carries out the AD translation of the output signal of said CDS circuit, and the memory which outputs the data which memorized and memorized the output signal of said ADC circuit to a microcomputer, The microcomputer which supplies the phase control signal for controlling the phase of the sample pulse supplied to said CDS circuit based on the output signal of said memory to a sample pulse generating circuit, The sample pulse generating circuit which outputs the sample pulse supplied to said CDS circuit based on the phase control signal supplied from said microcomputer, The clamp pulse generating circuit which generates the clamp pulse which clamps direct current level field through [ except the reset pulse of the output signal of CCD supplied to said CDS circuit ], Correlation duplex sampling equipment characterized by having an output terminal linking directly to the CDS circuit which takes out an image pick-up signal.

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to correlation duplex sampling equipment required for the improvement in S/N of the image pick-up signal of CCD which is an optoelectric transducer in image pick-up equipment etc.

[0002]

[Description of the Prior Art] In order to remove the reset noise included in the image pick-up signal of CCD in image pick-up equipment etc. and to acquire the image pick-up signal of high S/N in recent years, importance is increasingly attached to correlation duplex sampling equipment.

[0003] Below, the conventional correlation duplex sampling equipment is explained. Drawing 4 shows the block diagram showing the configuration of the conventional correlation duplex sampling equipment. In drawing 4 , a clamp pulse generating circuit and 12 consist of sample pulse generating circuits, and 13 consists of [ 9 / CCD and 10 ] output terminals for a CDS circuit and 11.

[0004] About the correlation duplex sampling equipment constituted as mentioned above, the actuation is explained below, referring to drawing 5 .

[0005] Drawing 5 is the signal waveform diagram showing the operating state in the conventional correlation duplex sampling equipment shown in drawing 4 .

[0006] If first the light which does not have level variation in time as shown in CCD9 from a lens etc. at (a) of drawing 5 enters, CCD9 which is an optoelectric transducer will output the output signal with which the field through component which fixed direct current level and a fixed reset pulse mix besides a signal as shown in (b) of drawing 5 is contained to CDS10.

[0007] The clamp pulse which clamps the fixed direct current level except the

reset pulse of (b) of drawing 5 as shown in CDS10 at (c) of drawing 5 next is supplied from the clamp pulse generating circuit 11, and the sample pulse which carries out sample hold of the signal part of (b) of drawing 5 as shown in (d) of drawing 5 in addition is supplied from the sample pulse generating circuit 12. The output terminal 13 directly linked with CDS10 at this time outputs the signal which clamped by the direct current level except the reset pulse of the signal wave form of (b) of drawing 5 as shown by (e) of drawing 5 , and carried out sample hold of the signal part.

[0008]

[Problem(s) to be Solved by the Invention] However, with the above-mentioned conventional configuration, since the phase of the sample pulse supplied to a CDS circuit was immobilization when the phase of the output signal of CCD outputted to a CDS circuit by a temperature change etc. changes, it had the trouble that sample hold of the signal part of a CCD output signal could not always be carried out the optimal.

[0009] This invention solves the above-mentioned conventional trouble, the phase of the sample pulse supplied to a CDS circuit is optimized using memory and a microcomputer, and it aims at offering the correlation duplex sampling equipment which can acquire the image pick-up signal of high S/N.

[0010]

[Means for Solving the Problem] In order to attain this purpose the correlation duplex sampling equipment of this invention The CDS circuit which is a correlation duplex sampling circuit which processes the output signal of CCD and CCD which is a photoelectrical strange conversion child, The ADC circuit which carries out the AD translation of the output signal of a CDS circuit, and outputs it, and the memory which outputs the data which memorized and memorized the output signal of an ADC circuit to a

microcomputer, The microcomputer which outputs the phase control signal for controlling the phase of the sample pulse supplied to a CDS circuit based on the output signal of memory, The sample pulse generating circuit which outputs the sample pulse supplied to a CDS circuit based on the phase control signal outputted from the microcomputer, It is constituted by the output terminal linking directly to the clamp pulse generating circuit which outputs the clamp pulse supplied to a CDS circuit, and the CDS circuit which takes out an image pick-up signal.

[0011]

[Function] By the configuration which described this invention above, CCD outputs the output signal which carried out photo electric conversion to a CDS circuit, a clamp pulse generating circuit supplies the clamp pulse which clamps direct current level field through [ except the reset pulse of the output signal of CCD ] to a CDS circuit, and a sample pulse generating circuit supplies the sample pulse for carrying out sample hold of the phase of the beginning of the signal period of the output signal of CCD to a CDS circuit. A CDS circuit outputs the output signal of processed CCD to an ADC circuit, the AD translation of the ADC circuit is carried out, and memory memorizes the output signal of an ADC circuit to the address 1. Next, a microcomputer outputs the phase control signal to which only the phase angle theta of arbitration advances the phase of a sample pulse from the phase of the beginning of the output signal of CCD to a sample pulse generating circuit, and a sample pulse generating circuit supplies the sample pulse by which only the phase angle theta of arbitration went to the CDS circuit from the phase of the beginning of the output signal of CCD. A CDS circuit outputs the output signal of processed CCD to an ADC circuit, the AD translation of the ADC circuit is carried out, and memory outputs to a microcomputer the data

which memorized the output signal of an ADC circuit to the address 2, and were memorized to the address 1 and the address 2. The sample pulse to which the phase control signal to which only the phase angle theta of arbitration will advance the phase of a sample pulse to a sample pulse generating circuit more nearly further than this time if larger than the value which the microcomputer took the difference of the data of the address 1 and the address 2, and difference set as the microcomputer was outputted, and only the phase angle theta of arbitration advanced the phase of a sample pulse to the CDS circuit more nearly further than this time in the sample pulse generating circuit is supplied. Again, a CDS circuit outputs the processed output signal to an ADC circuit, and the AD translation of the ADC circuit is carried out. Memory eliminates the data of the address 1 memorized at present, writes the data of the address 2 in the address 1, and memorizes the output signal of the ADC circuit where the point was obtained when only the phase angle theta of arbitration advanced the phase of a sample pulse further from this time as data of the address 2. A microcomputer outputs a phase control signal to a sample pulse generating circuit until it is completed as the value set as the microcomputer by the difference of the data of the address 1 outputted from memory, and the address 2. Only the phase angle theta of arbitration advances the phase of the sample pulse which supplies a sample pulse generating circuit to a CDS circuit. A CDS circuit The output signal of processed CCD is outputted to an ADC circuit. An ADC circuit An AD translation is carried out, and memory updates the data of the address 1 and the address 2, and outputs data to a microcomputer. A microcomputer When completed as the value set as the microcomputer by the difference of the address 1 and the address 2, the phase control signal to a sample pulse generating circuit is stopped. A sample pulse generating circuit The sample

pulse to the CDS circuit generated when the phase control signal outputted from the microcomputer was stopped is continued and outputted, and it takes out from the output terminal which has linked the image pick-up signal with a CDS circuit directly.

[0012]

[Example] One example of this invention is explained below, referring to a drawing.

[0013] Drawing 1 shows the block diagram of the correlation duplex sampling equipment in the 1st example of this invention. CCD which outputs the signal with which 1 carried out photo electric conversion of the light to the electrical signal using the lens etc. in drawing 1 , The CDS circuit which is a correlation duplex sampling circuit where 2 processes the output signal of CCD, The ADC circuit where 3 carries out the AD translation of the output signal of a CDS circuit, the memory which outputs the data which 4 memorized the output signal of an ADC circuit and were memorized to a microcomputer, The microcomputer which supplies a phase control signal for 5 to control the phase of the sample pulse supplied to said CDS circuit based on the output signal of memory to a sample pulse generating circuit, The sample pulse generating circuit which outputs the sample pulse which supplies 6 to said CDS circuit based on the phase control signal supplied from the microcomputer, The clamp pulse generating circuit which generates the clamp pulse which clamps direct current level field through [ except the reset pulse of the output signal of CCD which supplies 7 to a CDS circuit ], and 8 are the output terminals linking directly to the CDS circuit which takes out an image pick-up signal.

[0014] The correlation duplex sampling equipment of this example constituted as mentioned above is explained referring to the drawing 2 of

operation and drawing 3 below. Drawing 2 and drawing 3 are the signal waveform diagrams showing the operating state of this operation.

[0015] First, if the light which does not have level variation in time as shown in CCD1 from a lens etc. at (a) of drawing 2 enters, from CCD1, the output signal with which the field through component which fixed direct current level and a fixed reset pulse mix besides a signal as shown in (b) of drawing 2 is contained will be outputted to CDS2. The clamp pulse which clamps direct current level field through [ except the reset pulse of the output signal of CCD as shown in (c) of drawing 2 from the clamp pulse generating circuit 7 ] is supplied to CDS2, and the sample pulse which carries out sample hold of the phase of the beginning of the signal period of the output signal of CCD as shown in (d) of drawing 2 from a sample pulse generating circuit is supplied. The output signal of CDS2 is outputted to ADC3, an AD translation is carried out by ADC3, the output signal of amplitude value A as shown in (g) of drawing 3 is outputted to memory 4, and it memorizes as data of the address 1 of memory 4. Next, the phase control signal which is a DC signal of amplitude value B as shown in (h) of drawing 3 from a microcomputer 5 is outputted to the sample pulse generating circuit 6. Based on the phase control signal outputted from the microcomputer 5, the sample pulse generating circuit 6 The sample pulse to which only theta 0 progressed from the phase of the sample pulse supplied to CDS2 of (d) of drawing 2 as shown in (e) of drawing 2 is again supplied to CDS2. The AD translation of the output signal of CDS2 is carried out by ADC3, the output signal of amplitude value C as shown in (i) of drawing 3 is outputted to memory 4, and it memorizes as data of the address 2 of memory 4. The data of the address 1 of memory 4 and the address 2 are outputted to a microcomputer 5. And a microcomputer 5 Since the signal of the amplitude value D which is the

difference which detected and detected the signal of the amplitude value D which is the differential signal of the data of the address 1 and the address 2 as shown in (j) of drawing 3 is larger than the value set as the microcomputer, The phase control signal which is a DC signal of amplitude value E as shown in (k) of drawing 3 is outputted to the sample pulse generating circuit 6. Based on the phase control signal outputted from the microcomputer 5, the sample pulse generating circuit 6 The sample pulse to which only theta 1 progressed further from the phase of the sample pulse supplied to CDS2 of (e) of drawing 2 as shown in (f) of drawing 2 is again supplied to CDS2. The AD translation of the output signal of CDS2 is carried out by ADC3. Memory 4 The data which had memorized the point to the address 1 are eliminated, the data of the address 2 are memorized as data of the address 1, and the output signal of the amplitude value F outputted from ADC3 as shown in (l) of drawing 3 is memorized to the address 2 of memory 4. The data of the address 1 of memory 4 and the address 2 are outputted to a microcomputer 5. A microcomputer 5 detects the signal of the amplitude value G which is the differential signal of the data of the address 1 and the address 2 as shown in (m) of drawing 3 . Since it was completed as the value set as the microcomputer by the signal of the amplitude value G which is the detected differential signal, the phase control signal to a sample pulse generating circuit is stopped. In a sample pulse generating circuit The sample pulse to the CDS circuit generated when the phase control signal outputted from the microcomputer was stopped is continued and outputted, and an image pick-up signal is taken out from the output terminal 8 linking directly to a CDS circuit.

[0016] According to this example, the phase of the sample pulse supplied to CDS2 is changed to arbitration as mentioned above. The output signal of

CCD1 processed by CDS2 obtained before and after the phase change of a sample pulse is memorized by memory 4. The phase of the sample pulse supplied to CDS2 until it is completed as the value set as the microcomputer 5 by the value is changed. the difference of the data memorized by memory 4 -- the difference of the data which detected the value with the microcomputer 5 and were detected with the microcomputer 5 -- When completed as the value set as the microcomputer by the value, the phase control to a sample pulse generating circuit is suspended. the difference of the data detected with the microcomputer 5 -- a sample pulse generating circuit The image pick-up signal of high S/N can be acquired by continuing and supplying the sample pulse to the CDS circuit generated when the phase control signal outputted from the microcomputer was stopped, and taking out an image pick-up signal from the output terminal 8 linking directly to CDS2.

[0017]

[Effect of the Invention] As mentioned above, this invention can acquire the image pick-up signal of high S/N in making the optimal based on the output signal of a CDS circuit the phase of the sample pulse supplied to a CDS circuit, when the phase of the output signal of the image sensors inputted into a CDS circuit by a temperature change etc. changes.

[Brief Description of the Drawings]

[Drawing 1] The block diagram of the correlation duplex sampling equipment in the 1st example of this invention

[Drawing 2] The signal waveform diagram for explaining the operating state of the correlation duplex sampling equipment in this example

[Drawing 3] The signal waveform diagram for explaining the operating state of the correlation duplex sampling equipment in this example

[Drawing 4] The block diagram showing the configuration of the conventional

correlation duplex sampling equipment

[Drawing 5] The signal waveform diagram for explaining the operating state of the conventional correlation duplex sampling equipment

[Description of Notations]

1,9 CCD

2 Ten CDS circuit

3 ADC Circuit

4 Memory

5 Microcomputer

6 12 Sample pulse generating circuit

7 11 Clamp pulse generating circuit

8 13 Output terminal